L Number	Hits	Search Text	DB	Time stamp
-	1	5437034.pn.	USPAT	2003/12/30 13:01
-	1	6226776.pn.	USPAT	2003/12/19 17:30
-	1	5600579.pn.	USPAT	2003/12/19 17:30
-	1	5774380.pn.	USPAT	2003/12/19 17:31
-	11	("5437034" US-6226776 US-5600579 US-5774380) and (HDL VHDL system simulation simulating simulate circuit model code coded coding storing store stored saved save saving recording record recorded executed hardware description language object code "C" programming program programmed)	USPAT	2003/12/27 22:37
-	208	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed)	USPAT	2004/01/03 18:59
-	74	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930"	USPAT	2003/12/27 22:40
-	74	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/27 22:40
-	62	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (convert converting converted compile compiling compiled)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/27 22:42
-	58	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (convert converting converted compile compiling compiled) and (clock clocking clocked cycle cycling)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/27 22:43
-	49	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (convert converting converted compile compiling compiled) and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/27 22:44
-	49	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (convert converting converted compile compiling compiled) and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/27 22:45
-	49	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (convert converting converted compile compiling compiled) and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/31 00:08

-	7	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (convert converting converted compile compiling compiled) and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming interface")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/27 22:49
-	7	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (convert converting converted compile compiling compiled) and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming interface")	USPAT	2003/12/27 22:54
-	7	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (convert converting converted compile compiling compiled) and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming interface")	USPAT	2003/12/27 22:55
-	9	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (convert converting converted compile compiling compiled) and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming interface")	USPAT	2003/12/28 21:46
-	4	(US-5600579-$ or US-5437034-$ or US-6226776-$ or US-5774380-$).did.	USPAT	2003/12/27 22:59
-	2	"60156732" "60/156,732" "60,156,732"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/27 23:00
-	0	("convert" "compile") adj "HDL" adj "to" adj "binary"	USPAT	2003/12/28 21:10
-	58	("convert" "compile") adj "HDL"	USPAT	2003/12/28 21:10
-	0	("convert" "compile") adj "HDL" same "binary"	USPAT	2003/12/28 21:10
-	22	("convert" "compile") adj "HDL" same code	USPAT	2003/12/28 21:11
-	18	("convert" "compile") adj "HDL" same code and @ad < "19990930"	USPAT	2003/12/28 21:37
-	0	("convert" "compile") adj "HDL" same binary and @pd < "19990930"	USPAT	2003/12/28 21:38
-	0	("convert" "compile") adj "HDL" same binary and @ad < "19990930"	USPAT	2003/12/28 21:38
-	2	("convert" "compile") adj "HDL" same machine and @ad < "19990930"	USPAT	2003/12/28 21:45

-	1	("convert" "compile") adj "HDL" same machine and @pd < "19990930"	USPAT	2003/12/28 21:45
-	9	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (convert converting converted compile compiling compiled) and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming interface")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/28 21:47
-	9	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming interface") and (convert converting converted compile compiling compiled) same (machine code binary assembly)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/28 21:55
-	4	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming interface") and (convert converting converted compile compiling compiled) adj4 (code binary assembly)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/28 22:08
-	9	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming interface") and (convert converting converted compile compiling compiled compiler compilers) and (code binary assembly machine)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/29 13:56
-	1	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19980930" and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming interface") and (convert converting converted compile compiling compiled compiler compilers) and (code binary assembly machine)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/29 13:57
-	0	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and 5437037.pn.	USPAT	2003/12/30 13:02

-	0	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and executed and object and "C" and (programming program programmed) and 5437037.pn.	USPAT	2003/12/30 13:03
-	0	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and "C" and (programming program programmed) and 5437037.pn.	USPAT	2003/12/30 13:03
-	1	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (programming program programmed) and 5437037.pn.	USPAT	2003/12/31 00:33
-	28	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19980930" and (convert converting converted compile compiling compiled) and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/31 00:09
-	17	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19980930" and (convert converting converted compile compiling compiled) and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and oriented	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/31 00:09
-	0	(HDL VHDL "hardware description language") near4 (compile compiled compiling convert converting converted convertion) near4 (assembly assemling assembled)	USPAT	2003/12/31 00:35
-	13	(HDL VHDL "hardware description language") same (compile compiled compiling convert converting converted convertion) same (assembly assemling assembled)	USPAT	2003/12/31 00:36
-	13	(HDL VHDL "hardware description language") same (compile compiled compiling convert converting converted convertion) same (assembly assemling assembled) and pd<19980930	USPAT	2003/12/31 00:36
-	1	(HDL VHDL "hardware description language") same (compile compiled compiling convert converting converted convertion) same (assembly assemling assembled) and @pd<19980930	USPAT	2003/12/31 00:40
-	2	(HDL VHDL "hardware description language") same (compile compiled compiling convert converting converted convertion) same (assembly assemling assembled) and @pd<19990930	USPAT	2003/12/31 00:44
-	4	((HDL VHDL "hardware description language") same (compile compiled compiling convert converting converted convertion) same (binary assembly assemling assembled) and @pd<19990930) and (HDL VHDL hardware description language compile compiling compiled compilation converting convert converted convertion binary assembling assembly)	USPAT	2003/12/31 12:40
-	380	"HDL" and "RTL"	USPAT	2003/12/31 12:40
-	306	"HDL" same "RTL"	USPAT	2003/12/31 12:40
-	141	"HDL" same "RTL" and ("binary" "assembly")	USPAT	2003/12/31 12:41
-	123	"HDL" same "RTL" and ("binary" "assembly") and interface	USPAT	2003/12/31 12:41
-	13	"HDL" same "RTL" and ("binary" "assembly") and interface and @pd< "19980930"	USPAT	2003/12/31 13:50
-	9538	Meyer.in.	USPAT	2003/12/31 13:51
-	0	Stven adj4 Meyer	USPAT	2003/12/31 13:51
-	1	Steven adj4 Meyer	USPAT	2003/12/31 13:51
-	147	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and procedur$	USPAT	2004/01/07 12:28

-	106	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and procedur$ and task$ and block$ and delay$	USPAT	2004/01/03 19:03
-	106	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and procedur$ and task$ and block$ and delay$ and control$ and (operation process)	USPAT	2004/01/03 20:13
-	22	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and procedur$ and task$ and block$ and delay$ and control$ and (operation process) and @pd<19980930	USPAT	2004/01/03 20:24
-	92	(HDL VHDL "hardware discription language" Verilog) and (PLI "programming language interface")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/06 14:36
-	6	@pd < "19980930" and (HDL VHDL "hardware discription language" Verilog) and (PLI "programming language interface")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/07 12:29
-	5	@pd < "19980930" and (HDL VHDL "hardware discription language" Verilog) and (PLI "programming language interface") and (C++ "C" "object-oriented language" "object oriented")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/06 14:40
-	4	@pd < "19980930" and (HDL VHDL "hardware discription language" Verilog) and (PLI "programming language interface") and (C++ "C" "object-oriented language" "object oriented") and (simulation simulated simulate simulating) and (binary object code assembly)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/06 14:41
-	1	@pd < "19980930" and (HDL VHDL "hardware discription language" Verilog) and (PLI "programming language interface") and (C++ "C" "object-oriented language" "object oriented") and (simulation simulated simulate simulating) and (binary assembly) and (object code)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/06 14:42
-	1	@pd < "19980930" and (HDL VHDL "hardware discription language" Verilog) and (PLI "programming language interface") and (C++ "C" "object-oriented language" "object oriented") and (simulation simulated simulate simulating) and (binary assembly)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/06 14:43
-	1	@pd < "19980930" and (HDL VHDL "hardware discription language" Verilog) and (PLI "programming language interface") and (C++ "C" "object-oriented language" "object oriented") and (simulation simulated simulate simulating) and (binary assembly) and (memory stored storing storage)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/06 14:43
-	0	@pd < "19980930" and (HDL VHDL "hardware discription language" Verilog) and (PLI "programming language interface")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/06 16:06

-	22	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and procedur$ and (simulat$ same binary)	USPAT	2004/01/07 12:29
-	1	@pd < "19980930" and (HDL VHDL "hardware discription language" Verilog) and (PLI "programming language interface") and (simulat$ same binary)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/07 12:50
-	0	(binary assembly) same "all simulator"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/07 12:52
-	0	(binary assembly) same "all simulators"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/07 12:52
-	0	(binary assembly) and "all simulators"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/07 12:52
-	6653	(binary assembly) and simulator	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/07 12:52
-	3378	(binary assembly) and simulator and @pd < "19980930"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/07 12:53
-	0	(binary assembly) and simulator and @pd < "19980930" and 703/*.ccls	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/07 12:54
-	335	(binary assembly) and simulator and @pd < "19980930" and "703"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/07 12:54
-	0	(binary assembly) and simulator and @pd < "19980930" and "703" and "all"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/07 12:55
-	1	(binary assembly) and simulator and @pd < "19980930" and "all"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/07 12:55